REMARKS

Applicant thanks the Examiner for the very thorough consideration given the present application.

Claims 1-6 are now present in this application. Claims 1, 2, 3 and 6 are independent.

Amendments have been made to the specification, and claims 1 and 3 have been amended and claim 6 has been added. Reconsideration of this application, as amended, is respectfully requested.

Priority Under 35 U.S.C. § 119

Applicant thanks the Examiner for acknowledging Applicant's claim for foreign priority under 35 U.S.C. § 119, and receipt of the certified priority document.

Information Disclosure Citation

Applicant thanks the Examiner for considering the reference supplied with the Information Disclosure Statement filed December 2, 1999, and for providing Applicant with an initialed copy of the PTO-1449 form filed therewith.

Drawings

Applicant has not received a Notice of Draftsperson's Patent Drawing Review PTO-948 indicating whether or not the formal drawings have been approved by the Draftsperson. Clarification in the next Office Action is respectfully requested.

Specification Objection

The Examiner has objected to the specification because of several informalities. In order to overcome this objection, Applicant has amended the specification in order to correct the deficiencies pointed out by the Examiner. Reconsideration and withdrawal of this objection are respectfully requested.

Specification Amendments

Applicant has amended the specification in order to correct minor typographical errors, and to place the specification in better form.

Claim Objections

The Examiner has objected to claims 1 and 3 because of several informalities. In order to overcome this objection, Applicant has have amended

claims 1 and 3 in order to correct the deficiencies pointed out by the Examiner. Reconsideration and withdrawal of this objection are respectfully requested.

Rejection Under 35 U.S.C. § 102

Claim 1 stands rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,821,587 to Jeong, for the reasons set forth in paragraph 5 of the Office Action. This rejection is respectfully traversed.

Claim 1 has been amended. Jeong discloses a circuit in Fig. 1 having a resistor connected in series between a Control/Address PAD 100 and a transistor Q3. Applicant asserts that transistor Q3 is not a chip (integrated circuit), but a discrete component. A single discrete component does not comprise a chip.

Further, Fig. 1 of Jeong discloses a single resistor. That is, the resistor of Jeong is not connected in parallel with other resistors. Therefore Jeong does not disclose a plurality of transistors, each connected between the pad and the main chip, said transistors having a plurality of resistors connected to an input terminal, said resistors being connected in parallel with each other, and having no resistor connected between said transistors and ground, as recited in independent claim 1, as amended. Reconsideration and withdrawal of this art grounds of rejection are respectfully requested.

Rejections under 35 U.S.C. §103

Claims 2-5 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Jeong, for the reasons set forth in paragraph 6 of the Office Action. This rejection is respectfully traversed.

The Examiner admits that Fig. 5 of Jeong does not disclose a buffered layer formed on the first insulating film inclusive of the first contact hole and electrically connected to the input terminal for acting as a resistor. To fill this vacancy, the Examiner asserts that it would have been obvious to one of the ordinary skill in the art to use a buffered layer beneath the input pad 43 on the first insulating film in order to make a resistor in contact with the input pad.

Jeong discloses a metal layer 39, formed on the first insulating film, inclusive of the first contact hole and electrically connected to the input terminal (drain). This metal layer is formed in the exact place where the Examiner asserts that one of ordinary skill in the art would be motivated to use a resistor. A conductor promotes the flow of current. A resistor restricts the flow of current. These concepts are diametrically opposed. Therefore, Jeong, which uses a metal conductive layer instead of a resistor or a resistive buffer layer, teaches away from using a resistor, such as the resistor disclosed in Fig. 1 of Jeong. Applicant asserts that there is no motivation to substitute a resistor in the place where a pure conductor is required.

Therefore, Jeong does not disclose or suggest a buffered layer formed on the first insulating film inclusive of the first contact hole and electrically connected to the input terminal for acting as a resistor, as recited in independent claim 2, and similarly stated in independent claim 3.

Claims 4 and 5, dependent on claim 3, are patentable for at least the reasons stated with respect to independent claim 3. Reconsideration and withdrawal of this art grounds of rejection are respectfully requested.

Added Claims

Independent Claim 6 has been added for the Examiner's consideration. Independent claim 6 recites a combination of elements in an ESC (Electro-Static-Discharge) protection circuit including a pad and a main chip, said chip comprising more than one discrete component. Applicant respectfully submits that this combination of elements as set forth in independent claim 6, is not disclosed or made obvious by the prior art of record.

Consideration and allowance of claim 6 are respectfully requested.

Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance.

If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone Percy L. Square, Registration No. 51,084 at (703) 205-8034, in the Washington, D.C. area.

Prompt and favorable consideration of this Amendment is respectfully requested.

Attached hereto is a marked-up version of the changes made to the application by this Amendment.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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Attachment: Version with Markings to Show Changes Made

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

The paragraph beginning on page 1, line 7, has been amended as follows:

--Fig. 1 illustrates a system of a related art ESD protection circuit. In general, a maximum field strength against which an oxide film in an MOS transistor can endure is 6MV/cm, which corresponds to 30V if the oxide film is scaled up to a thickness of 50nm. A voltage of this [range] magnitude can be easily generated from [a] minute static electricity [occurred] occurring around a circuit [with easy]. There is [ceaseless] continuous generation of static electricity when a human body makes movement, and the human body acts as a carrier that carries a great amount of charge. Therefore, if the human body comes [closer] close to a conductor, the static electricity is discharged, causing a great amount of current to flow within a short time. Thus, as [an] the amount of charge [that can break the] required to damage a transistor is very small, an ESD protection circuit 2 is provided to an input pin between a pad 1 and a main chip 3 so that the static electricity, rushing into an inner part of the main chip 3, is discharged through an appropriate circuit for maintaining voltages on an input terminal and an output terminal within fixed ranges. Thus, an input protection circuit and an output protection circuit are required for prevention of static breakdown.--

The paragraph beginning on page 2, line 23, has been amended as follows:

--Referring to Fig. 2, the first exemplary related art ESD protection circuit is provided with a plurality of first transistors 11 each having a collector

connected to an input pin between a pad 1 and a main chip 3, and a gate and an emitter both grounded, wherein a voltage from the pad 1 is provided to the main chip 3 directly in a regular case and an inflow of a static electricity is bypassed to the [first] transistors 11, thereby protecting the main chip 3.--

The paragraph beginning on page 3, line 5, has been amended as follows:

--Referring to Fig. [2] 3, the second exemplary related art ESD protection circuit is provided with a plurality of second transistors 12 each having a collector connected to an input pin between a pad 1 and a main chip 3 through a first resistor [21] 13, a gate grounded, and an emitter grounded through a second resistor [22] 14, wherein a voltage from the pad 1 is provided to the main chip 3 directly in a regular case and an inflow of [a] static electricity is bypassed to the [second] transistors 12, thereby protecting the main chip 3.--

The paragraph beginning on page 3, line 13, has been amended as follows:

--First, the related art ESD protection circuit, having the plurality of [first] transistors each with the collector connected to the input pin between the pad and the main chip and the gate and the emitter both grounded, i.e., no resistor is connected to the emitter/collector, may be [involved in occurrence of] subject to breakage [of] at a particular point caused by momentary concentration of a charge on the particular point in a case of a BJT of [a] single or plural units or in [a] case the static electricity is [occurred] generated from inside, and a space of the ESD protection circuit for preventing such [a] an occurrence requires a larger area.--

The paragraph beginning on page 3, line 20, has been amended as follows:

--Second, the related art ESD protection circuit, having the plurality of [the second] transistors each with the collector connected to the input pin between the pad and the main chip through the first resistor, the gate grounded, and the emitter grounded through the second resistor, is involved in [a] reduction of [a] BJT gain caused by the two resistors connected to the emitter /collector and a drop of an ESD capability.--

The paragraph beginning on page 6, line 18, has been amended as follows:

--Referring to Fig. 5, the ESD protection circuit of the present invention includes an NMOS transistor 42 formed on a semiconductor substrate 41, a first ILD (InterLayer Dielectric) layer 43 formed on the semiconductor substrate 41 inclusive of the NMOS transistor 42 and having a first contact hole to a drain of the NMOS transistor 42, a buffered layer 44 formed on the ILD layer 43 inclusive of the first contact hole and electrically connected to the drain for acting as a resistor, a second ILD layer [43] 45 formed on the first ILD layer 43 inclusive of the buffered layer 44 and having a second contact hole to the buffered layer 44, and a pad 1 formed on the second ILD layer 45 inclusive of the second contact hole and electrically connected to the buffered layer 44, for discharging [a] static electricity through the pad 1, the buffered layer 44, the drain of the NMOS transistor 42, and the source of the NMOS transistor 42.--

The paragraph beginning on page 7, line 7, has been amended as follows:

--Referring to Fig. 6a, the method for fabricating an ESD protection circuit in accordance with a preferred embodiment of the present invention starts with forming an NMOS transistor 42 on a semiconductor substrate 41. As shown in Fig. 6b, a first ILD layer 42 and a first photoresist film are formed on the semiconductor substrate 41 inclusive of the NMOS transistor [42] 43,

and subjected to selective exposure and development to remove only a portion of the first photoresist film in which a first contact hole to a drain of the NMOS transistor 42 is to be formed. The selectively exposed and developed first photoresist film is used as a mask in etching the first ILD layer selectively, to form a first contact hole, and, then, the first photoresist film is removed. Polysilicon and a second photoresist film are formed on the first ILD layer 43 inclusive of the first contact hole, and the second photoresist film is subjected to selective exposure and development to leave the second photoresist film only on a region on which a buffered layer is to be formed. In this instance, instead of the polysilicon, a silicide may be used. The selectively exposed and developed second photoresist film is used as a mask in etching the polysilicon selectively, to form a buffered layer 44, and, then, the second photoresist film is removed. As shown in Fig. 6c, a second ILD layer 45 and a third photoresist film are formed on the first ILD layer 43 inclusive of the buffered layer 44, and the third photoresist film is subjected to selective exposure and development to remove a portion of the third photoresist film in which a second contact hole to the buffered layer 44 is to be formed. The selectively exposed and developed third photoresist film is used as a mask in selective etching of the second ILD layer 45, to form a second contact hole, and, then, the third photoresist film is removed. Then, a pad 1 is formed on the second ILD layer 45 inclusive of the second contact hole.--

The paragraph beginning on page 8, line 5, has been amended as follows:

--Because the ESD protection circuit of the present invention has a plurality of transistors each with a collector only connected to an input terminal through a resistor, connected to an input pin between a pad and a main chip, and a gate and an emitter both grounded, the ESD protection circuit and the method for fabricating the same is favorable for use in a fast

speed device which should have a small input capacitor, because the resistor at the input terminal increases a secondary breakdown voltage and distributes [an] static electricity so as not to concentrate on a particular point, the particular point breakage can be prevented, and because the ESD protection circuit of the present invention has a BJT gain greater than the related art ESD protection circuit having resistors connected both to the emitter/the collector, an ESD protection capability is improved.--

In the Claims:

The claims have been amended as follows:

1. (Amended) An ESC (Electro-Static-Discharge) protection circuit comprising:

a pad and a [maim] main chip; and,

a plurality of transistors, each connected between the pad and the main chip, said transistors [and] having a plurality of [a resistor] resistors connected [only] to an input terminal, said resistors being connected in parallel with each other, and having no resistor connected between said transistors and ground.

[2.]3. (Amended) A method for fabricating an ESD protection circuit, comprising the steps of:

(1) forming a transistor on a substrate;

(2) forming a first insulating film on the substrate inclusive of the transistor and having a first contact hole to an input terminal of the transistor;

(3) forming a buffered layer in the first contact hole and the first insulating film in the vicinity of the first contact hole;

(4) forming a second insulating film on the first insulating film inclusive of the buffered layer and having a second contact hole to the buffered layer;

and,

(5) forming a pad both on the second contact hole and the second insulating film in the vicinity of the second contact hole.

Claim 6 has been added.